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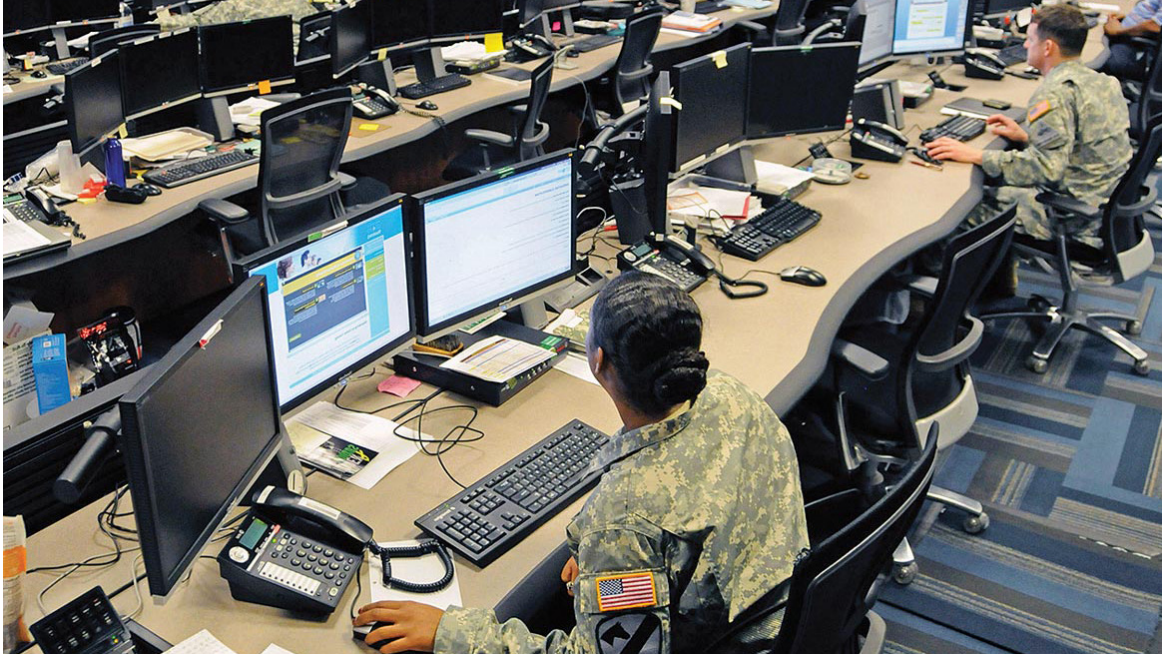
INTRODUCTION

Bill Wong
Editor,
Senior Content
Director

RUGGED, MILITARY AND AVIONIC SYSTEMS are much more complex these days and building from COTS hardware is the only way to do this quickly and efficiently. In the past, COTS often meant more custom than off-the-shelf. There were standards such as slot size but the interfaces and software protocols were not set. This made it difficult to interface systems as well as provide upgrade or replacement paths as each new iteration required significant redesign.

The Sensor Open Systems Architecture (SOSA) is the current culmination of the move to standardize as much of the hardware and software framework to make it easier for vendors to provide hardware and software that is closer to what the final system will require thereby minimizing the amount of customization developers need to do to get the systems to work for their particular application. SOSA does not define new standards but chooses from existing standards like OpenVPX. It also selects subsets of standards to further refine the standards that systems will be built on. This allows vendors to concentrate on delivering systems that have fewer requirements as well as developers that have fewer choices making it easier to come up with an optimal configuration based on these standards.



CHAPTER 1:

SOSA and VITA: Working Together for Next-Gen Defense Systems

RODGER HOSKING, Vice-president, Pentek, Inc.

The SOSA™ (Sensor Open Systems Architecture) Consortium is developing common open standards for designing, building, and deploying hardware, software, and firmware components of new military electronic systems. SOSA contributing members are U.S. government organizations including the U.S. DoD, Army, Navy, and Air Force, as well as key representatives from industry and universities.

SOSA adopts the most appropriate subsets of existing open standards to form a multi-purpose backbone of building blocks for current and future embedded systems for Radar, EO/IR, SIGINT, EW, and communications.

Objectives include vendor interoperability, lower procurement costs, easier new technology upgrades, quicker reaction to new requirements, and longer life cycles.

Because the emerging SOSA hardware standard draws primarily from OpenVPX and other related VITA standards, the new technologies, topologies, and environmental requirements critical to meeting SOSA objectives must be supported by extensions to these VITA standards.

This article is an overview of the SOSA and VITA organizations and how they interact, along with the challenges, successful strategies, and illustrative examples.

VITA Background & Mission

Introduced to the market in 1981, the VMEbus architecture began gaining market presence with specification development and products from Motorola and other early vendors, who formed the VMEbus Manufacturers Group (now VITA) in 1983.

In 1985, VITA (VMEbus International Trade Association) was founded to promote VMEbus in worldwide markets, and published its first directory of 174 vendor companies and over 2,700 product families. VMEbus soon won widespread acceptance and adoption

by defense, government, research, and industrial customers.

The VITA Technical Committee, formed in 1987 to develop dozens of new extensions to VMEbus, evolved in 1994 into the present day VITA Standards Organization (VSO). A year earlier, VITA became an accredited standards development organization with the American National Standards Institute (ANSI).

To overcome performance limitations of the parallel bus backplane of VMEbus, in 2003 VITA introduced the VITA 46 VPX standard to take advantage of new gigabit serial interconnect technology for 3U and 6U boards. In 2010, after widespread use, refinements, and serious interest in VPX for long-term defense programs, VITA announced the VITA 65 OpenVPX system specification, quickly ratified by ANSI.

VITA continues its strong role in promoting and developing open architecture embedded system standards, actively supporting numerous working groups in the VSO, and working with vendors and other organizations to embrace new technology and meet new market requirements.

Open Systems Architecture Directive and Initiatives

In May 2013, the U.S. Under Secretary of Defense issued a milestone memo mandating that all acquisition activity must incorporate DoD Open Systems Architecture (OSA) principles and practices. These include using existing or evolving open standards for well-defined modular hardware and software components that can be sourced from multiple vendors. Once proven, hardware platforms should be reusable for quick-reaction mission needs, feature upgrades, and new technology insertion. Software architectures must be layered and extensible to permit operating system and security upgrades, and to accommodate new applications and user interfaces. These advantages reduce development risks and help ensure significantly longer operational life-cycles.

In response, each of the three primary U.S. service branches (Army, Navy, and Air Force), began developing standards that embraced OSA principles to meet future procurement needs of deployed systems for their respective services.

The Army's CCDC (Combat Capabilities Development Command) in Aberdeen, MD developed CMOSS (C4ISR/EW Modular Open Suite of Standards). These standards include OpenVPX for hardware, VICTORY to share vehicle services (like time and position) for C4ISR/EW interoperability, and MORA (Modular Open RF Architecture) to share antennas and amplifiers. It also uses REDHAWK and SCA software frameworks.

The Navy's NAVAIR (Naval Air Systems Command) in Patuxent River, MD created HOST (Hardware Open Systems Technology), which initially focused on embedded processing for airborne and ground vehicle missions. Its major goal of abstracting hardware and software components aligned well with OSA concepts. HOST hardware definitions include three tiers: Tier 1 defines the deployed platform (airframe, vehicle, UAV, etc.), Tier 2 defines the embedded system enclosure, and Tier 3 the boards, backplanes, modules, and faceplates. Tiers 2 and 3 are subsets of OpenVPX modules and profiles. A registry of Tier 3 products offers an approved catalog of components for sharing across programs.

The Air Force's OMS (Open Mission Systems) initiative incorporates SOA (Service Oriented Architecture) for commercially developed concepts and middleware, and UCI (Universal Command and Control Interface), which standardizes massages and middleware for sharing command and control mission information between airborne system elements. OMS strongly embraces FACE (Future Airborne Capability Environment), a consortium of

The Open Group that adopts open software standards for avionics systems, which gained full support of all three armed services.

SOSA Consortium

While each service made significant progress in advancing OSA principles, they did so through different initiatives that often shared common open standards, including OpenVPX and FACE. However, each initiative also included specific mandates tailored for service-specific platform requirements.

After recognizing these facts, administrators within DoD and each of the services perceived a strong need to promote a single, common initiative to define acquisition activities across all three services.

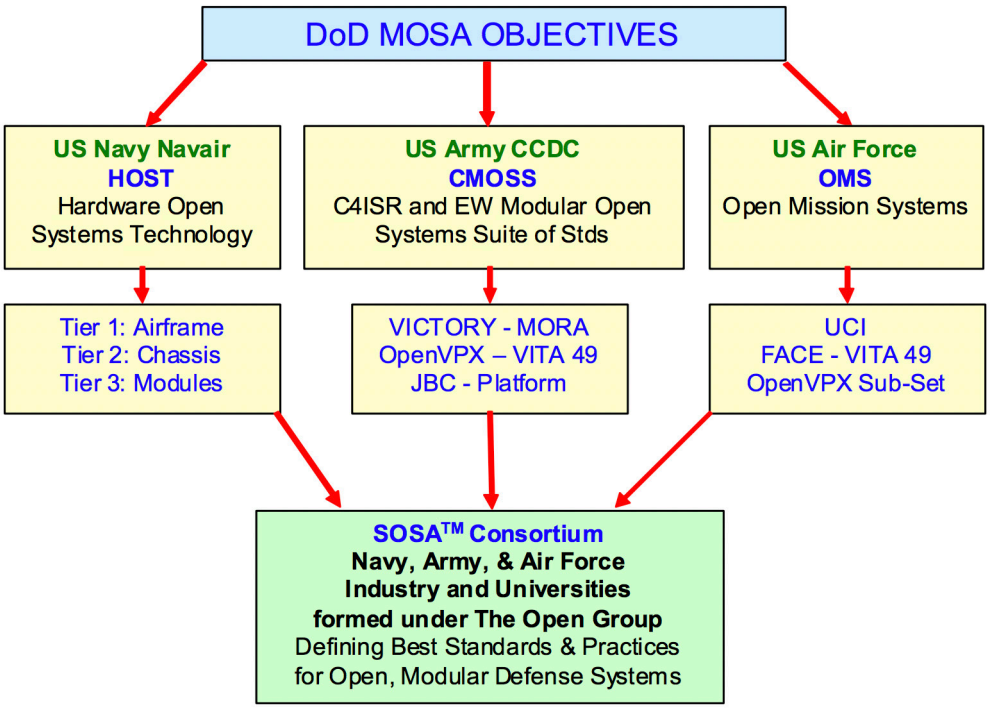


Figure 1. After independently developing standards in response to DoD MOSA objective each of the three services joined the SOSA Consortium to develop a unified standard.

In early 2017, the DoD issued an SBIR solicitation for Sensor Open System Architecture (SOSA) Architectural Research outlining the numerous OSA initiatives and objectives for a unified solution. This resulted in the formation of the SOSA Consortium managed by The Open Group, a large organization with strict and well-defined practices, policies, and procedures for standards development efforts.

A primary mandate of the SOSA Consortium is broad participation, commitment, and contribution from DoD, Army, Navy, and Air Force, as well as industry, academia, and other government organizations. Major objectives include development and adoption of open systems architecture standards for C4ISR to provide a common, multi-purpose backbone for radar, EO/IR, SIGINT, EW and countermeasure systems. Additional objectives include platform affordability, rapid fielding, re-configurability, new technology insertion, extended life-cycles, and re-purposing of hardware, firmware, and software.

Inside the SOSA Consortium

The SOSA Consortium Organization consists of two primary groups. The Business Working Group (BWG) defines business and acquisition practices, and creates guidance for acquisition programs. The Technical Working Group (TWG) is responsible for defining the SOSA Architecture, and producing the SOSA Technical Standard and SOSA Reference Design.

The SOSA Architecture presents a modular system structure, with tight integration within modules for encapsulating functionality and behaviors, and yet well-defined interfaces. These modules must be based on open, published standards, with consensus-based

influence stakeholders directing the evolution, and a strict conformance validation process. The SOSA Architecture protects IP (intellectual property) within the modules to incentivize innovation and competition.

The SOSA Technical Standard documents the SOSA Architecture with detailed rules and requirements drawn and adapted from a collection of open standards. The primary standards defining specifications for plug-in cards, backplanes, chassis, electrical components, and mechanical structures are VITA standards.

The SOSA Conformance Policy, now being defined by the SOSA Conformance Standing Committee, will define processes for qualifying products against the Technical Standard. They include multiple conformance verification processes, a single conformance certification process, and a single SOSA certified conformant product registration process. Until the award of certification, no product can claim to be SOSA conformant.

Membership in SOSA is restricted to US citizens and organizations so that DoD-sensitive or classified requirements can be presented by representatives from the armed services to promote solution strategies within the SOSA Technical Standard. For this reason, technical details of on-going discussions in the SOSA Technical Working Group may not be disclosed to the public. Once the standard is approved and released to the public, it will contain only specifications and rules, free from the underlying, sensitive use drivers.

VITA and SOSA

Because VITA is so central to the SOSA hardware definition, many of the same individuals in the SOSA TWG are also active participants in the VITA Standards Organization (VSO). Because restrictions on technical disclosures imposed on the TWG by SOSA do not apply to VSO, members of VSO must be mindful against referencing on-going SOSA technical topics in their VSO discussions and publications.

Nevertheless, the TWG does release period "snapshots" of the evolving SOSA Technical Standard that are publicly available for review, the latest being Snapshot 2 released in January 2020. While no conformance to these snapshots may be claimed, they illustrate the direction and underlying principles guiding the final standard.

In some cases, SOSA adopts only carefully selected subsets of existing VITA specifications. For example, the TWG adopted only a handful of the more than one hundred 3U and 6U OpenVPX slot and module profiles, based on an analysis that they could accommodate the majority of system requirements.

User-defined backplane pins defined in OpenVPX pose a nemesis for standardization efforts because they allow custom assignment of signals with interface standards, directions, and voltages. Profiles with user-defined pins are being deprecated in SOSA.

Figure 2. Rear view of 3U OpenVPX Module with two VITA 67.3D backplane connectors, each with 10 coaxial RF signals and 24 optical lanes. Courtesy TE Connectivity

Instead, work is underway to assign a minimum set of specific I/O standards to each group of legacy user-defined pins for each of the OpenVPX control, data, and expansion planes.

SOSA restricts the primary VPX power supplies to +12V only, prohibiting +5V, and +3.3V. This greatly simplifies the previous OpenVPX issue of balancing among three voltages to simplify chassis power supplies and standardize the plug-in cards.

Unlike most OpenVPX systems, SOSA requires hardware platform management leveraging the HOST 3.0 system management architecture, which itself is highly leveraged from VITA 46.11. A system manager module accesses all SOSA system elements for census taking, health monitoring, trouble shooting, new firmware/software upgrades, and reset/recovery operations.

Backplane I/O for RF signals and optical interfaces in OpenVPX have gained significant traction in CMOSS, MORA, and HOST systems over the last six years, all enabled by VITA 66 and VITA 67 specifications. Eliminating front panel cable harnesses wins high scores for maintenance and reliability. Some of the latest modular backplane standards offer extremely high density and even mixed RF/optical interfaces as shown in **Figure 2**.

In summary, when critical needs arise from SOSA customers (DoD services), SOSA TWG members can promote innovation for new standards within the VSO to accommodate them, while still complying with SOSA restrictions.

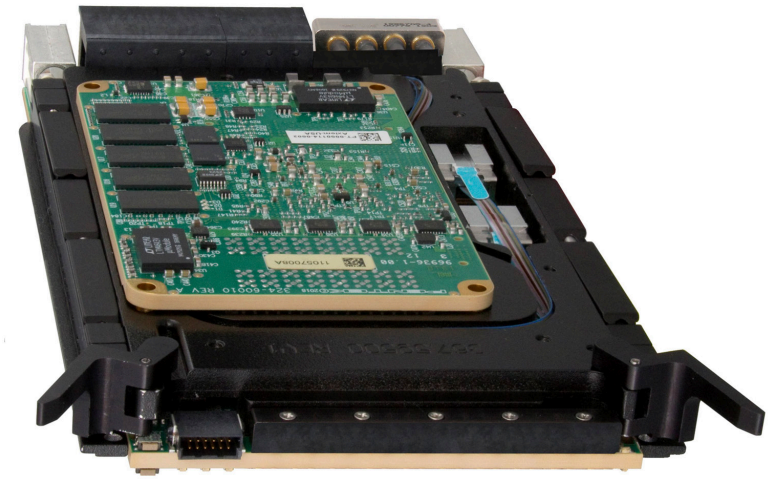


Figure 3. Pentek Quartz Model 5550 3U VPX 8 Channel A/D and D/A RFSoC SOSA-Aligned Processor incorporates RF and optical backplane using VITA 66 or VITA 67 connectors. Top cover removed to show details.

Next Steps

The release of the Technical Standard Snapshot 3 is scheduled for early second quarter 2020, but the current public health crisis may delay this because of cancellations of face-to-face meetings. Nevertheless, web-based conferencing will augment the regular on-going conference calls to help maintain the momentum.

It is expected that the release of the SOSA Technical Standard 1.0 will be completed about nine months after Snapshot 3. At that point, product vendors may begin the processes leading to full certification.

Nevertheless, vendors are now offering products that were “developed in alignment with SOSA” like the one shown in **Figure 3**. A key difference in the SOSA architecture from earlier open standards is the well-defined protection of IP, which encourages numerous examples of supplier innovation and investment.

The DoD is now issuing requests for proposals and information clearly favoring respondents that offer OSA-based solutions. The active participation in SOSA by the DoD, all three armed services, embedded industry vendors, universities, and research facilities gives evidence of their substantial commitments of resources and personnel. These clear signals ensure that SOSA is well on its way to revolutionize the future of embedded military electronics systems.

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CHAPTER 2:

SOSA, CMOSS, HOST, and Military Open Standards

BILL WONG, Editor

FACE, HOST, SOSA, CMOSS... sounds like military alphabet soup. However, this taste of standards is a good one.

Creating standards tends to be long and difficult process, but it enables the reduction of C4ISR system size, weight, and power (SWaP) and ensures commonality across multiple platforms by making it possible to share hardware and software components. It allows additional standards to be built on top of those, which is what the various military-related consortiums are doing to improve interoperability, as well as reduce development, deployment, and costs. On top of that, advanced systems can be delivered more quickly using the latest technology.

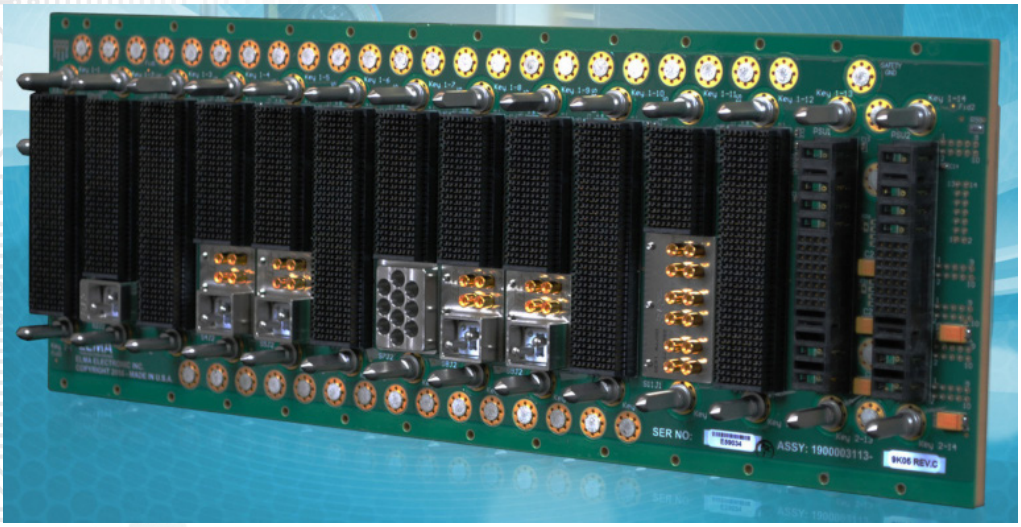
Some of these higher-level standards include Future Airborne Capability Environment (FACE), Sensor Open System Architecture (SOSA), Hardware Open Systems Technologies (HOST), and C4ISR/EW Modular Open Suite of Standards (CMOSS).

The Open Group hosts many of the standards, including those from the FACE and SOSA Consortiums. SOSA was initiated by the U.S. Air Force's Life Cycle Management Center (AFLCMC) at Wright-Patterson AFB in Ohio and incubated in the FACE Consortium in 2015.

The HOST standard was initiated by the U.S. Navy's Naval Air Systems Command (NAVAIR) at Patuxent River in 2014. HOST has been used in the integrated core processor (ICP) for the joint strike fighter (JSF) F-35, as well as for its panoramic cockpit display electronic unit (PCDEU).

CMOSS was started by the U.S. Army's Communications-Electronics Research, Development and Engineering Center (CERDEC) at Aberdeen Proving Grounds in 2013. It's designed to bring about the reduction of C4ISR SWaP in embedded military systems while ensuring commonality across multiple platforms through sharing of hardware and software components.

CMOSS currently incorporates the Vehicular Integration for C4ISR/EW Interoperability



1. OpenVPX backplanes like this one from Elma Electronic are the basis for military COTS standards.

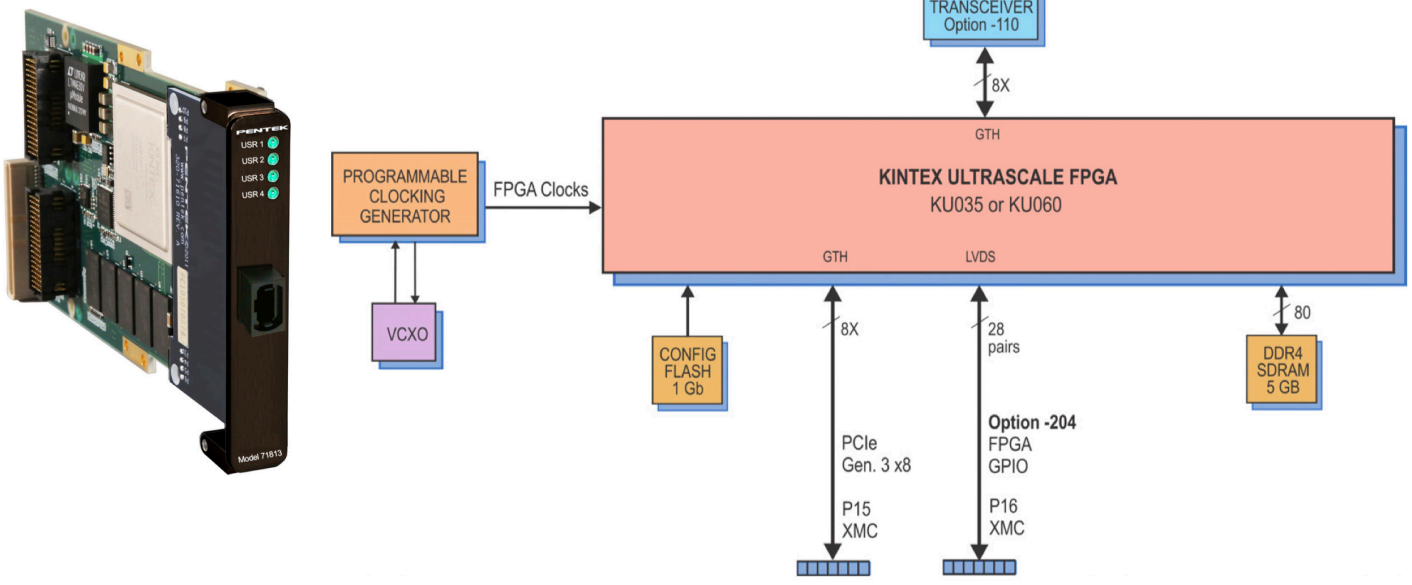
(VICTORY) standard that provides network-based interoperability using share services such as Time and Position and OpenVPX **(Fig. 1)**, a hardware form factor for fielding capabilities such as cards in a common chassis. Also included are the Modular Open RF Architecture (MORA) for driving functional decomposition to share resources like antennas and amplifiers and software frameworks that include REDHAWK, the Software Communications Architecture (SCA), and Future Airborne Capability Environment (FACE) to enable software portability.

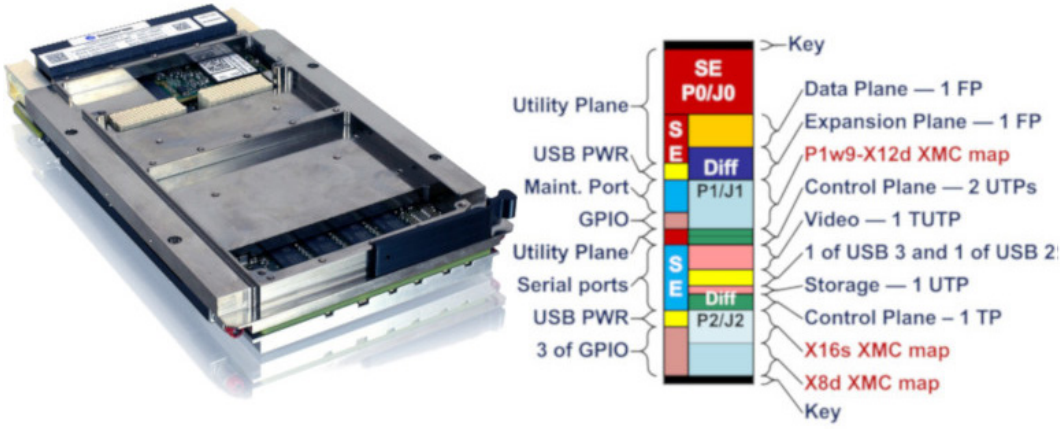
The idea for all of these standards is not to have just one part of the system compatible with a number of boards. It's also that these compatible boards work together, providing more options as well as simplifying system design and upgradability.

Kontron's VX305C-40G 3U VPX server blade **(Fig. 2)** is designed to handle SOSA-compatible XMC modules. The board has a 12-core Intel Xeon D with up to 32 GB of DDR4 ECC memory. It has a 40G Ethernet data plane and dual 10G Ethernet ports. The x8 PCI Express (PCIe) XMC slot is for the SOSA XMC module. It supports the I/O Intensive slot definition (SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16).

The SOSA OpenVPX standard backplane definitions specify how XMC modules would

2. The I/O Intensive definition (SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16) is on shown on the right.





3. SOSA modules like Pentek's Model 71813 XMC module (left) are designed to work with OpenVPX-compatible VPX boards that provide standard connections to the backplane.

connect through a compatible carrier board. An example is Pentek's Model 71813 XMC module (**Fig. 3**) that's built around the Xilinx Kintex Ultrascale FPGA. The Option -204 includes the P16 XMC connector with 28 pairs of LVDS connections to the FPGA for custom I/O. In addition, there's a front-panel MPO optical connector option supporting four 12-Gb/s lanes to the FPGA.

The SOSA standard also defines compute-intensive slots (**Fig. 4**): the Primary RF/Compute Intensive (SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-0) (left) and a Secondary RF/Compute Intensive (SLT3-PAY-1F1U1S1S1U1U4F1J-14.6.13-0) (right) slot interface.

In theory, compatible boards could be swapped in and out with only software changes. Having standard backplanes and XMC interfaces allows for easier specification of development projects as well as specifying upgrades and replacements. While backplanes will remain custom, their design should be greatly simplified since a more limited subset of OpenVPX possibilities can be employed.

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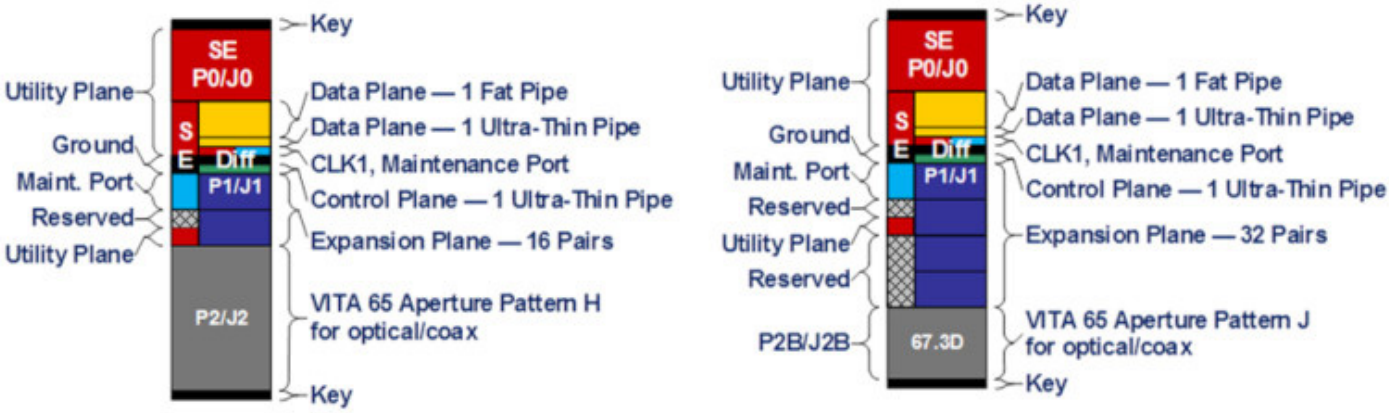

4. SOSA also defines a Primary RF/Compute Intensive (SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-0) (left) and a Secondary RF/Compute Intensive (SLT3-PAY-1F1U1S1S1U1U4F1J-14.6.13-0) (right) slot interface.

CHAPTER 3:

Military-Service Research Builds Layered Standards on COTS Hardware

BILL WONG, Editor

Looking for ways to cut software costs, a combined service research effort is delivering standards such as HOST, CMOSS, and SOSA.

Military and avionics systems often require custom solutions because of their cutting-edge requirements. The trend to use commercial off-the-shelf (COTS) systems is intended to expand the number of options available to designers while reducing costs. The VITA VPX standards address much of this in terms of hardware, but these days software costs are often greater.

On that front, the three U.S. service research groups—Army CERDEC, Air Force AFLCMC, and Navy NAVAIR—have been working on additional hardware and software standards. These are now being integrated to provide common frameworks that can be used to acquire new materials and software **(Fig. 1).** Though the alphabet soup of projects is large, they're all being built on industry standards like VPX.

Still, the new standards face significant integration challenges, including competition for limited platform resources; redundant subsystem components; complex, costly and weighty cabling; excessive heat generation; and less space on the platform for soldiers. There are major RF compatibility concerns, too, due to the large number of diverse systems already in the field. Likewise, the high cost of maintaining and upgrading systems must be addressed.

One central project is the C4ISR/EW Modular Open Suite of Standards (CMOSS). It's an aggregate of many existing projects plus new and existing standards such as Vehicular Integration for C4ISR/EW Interoperability (VICTORY), Modular Open RF Architecture (MORA), OpenVPX, REDHAWK, Software Communications Architecture (SCA), and the Open Group's Future Airborne Capability Environment (FACE). NAVAIR's Hardware Open Systems Technology (HOST) is also part of the mix, although a segment of the overall

design-integration process will merge HOST and CMOSS. CMOSS is now part of, and managed under, the Sensor Open Systems Architecture (SOSA).

The systems take a layers approach, building on existing hardware and software standards like OpenVPX and Data Distribution Service (DDS). The end game for SOSA **(Fig. 2)** is "delivery of a set of technical and business reference architectures, IP business case, an acquisition strategy document, and a tailorable request for proposal (RFP) technical package."

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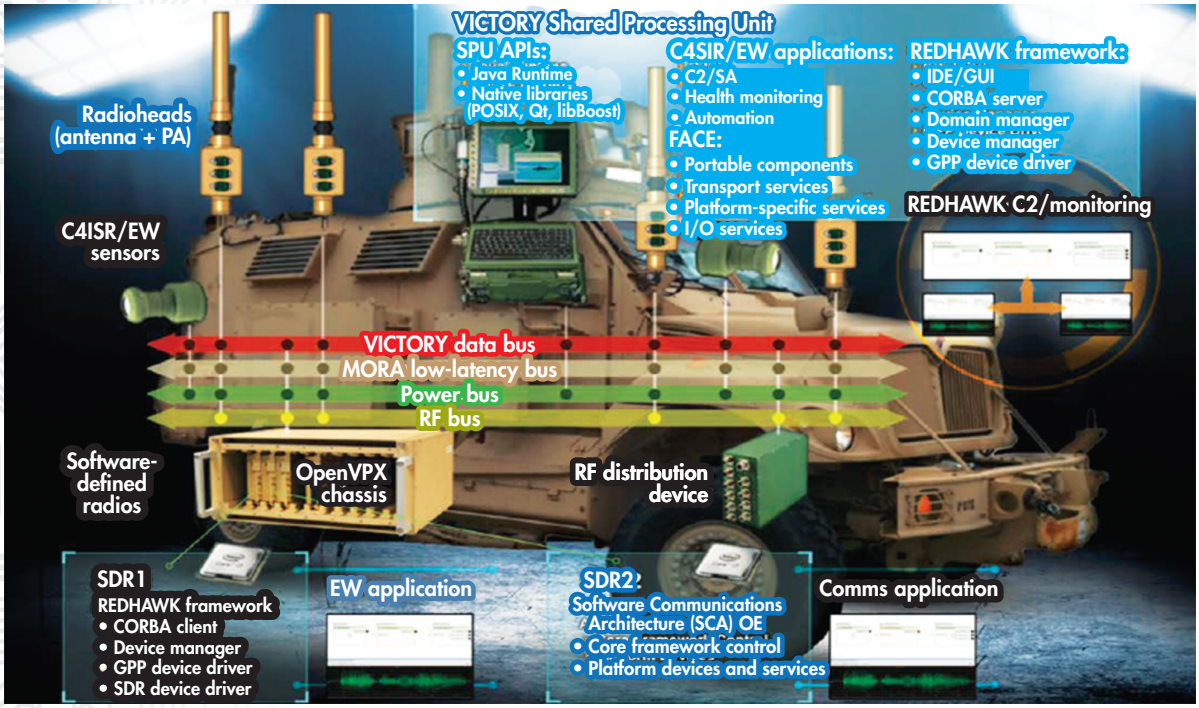
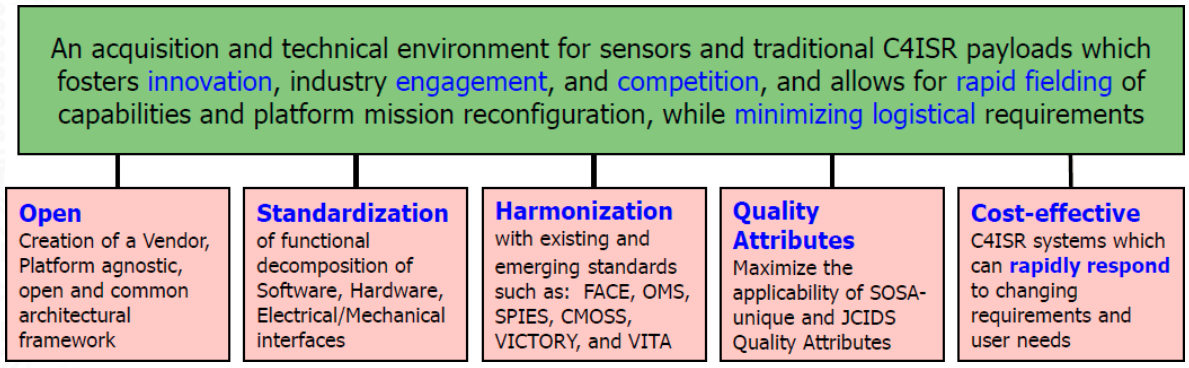
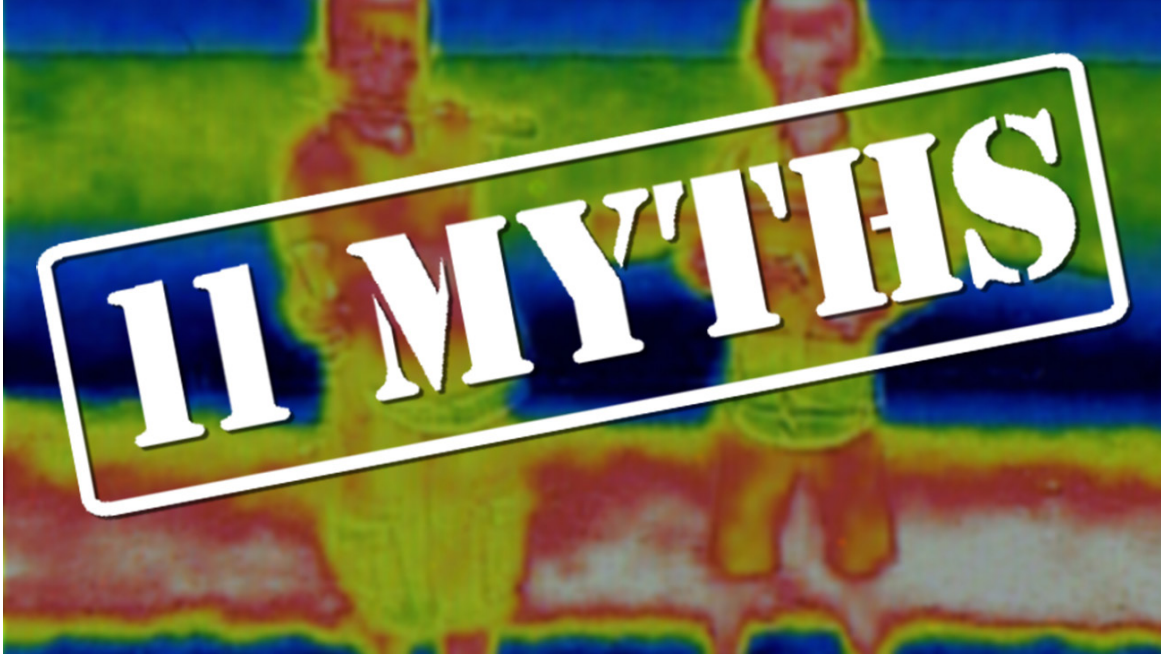


1. Multiple, layered standards including CMOSS and SOSA are being applied to new systems design for military applications.



2. The Sensor Open Systems Architecture (SOSA) group intends to deliver a set of technical and business reference architectures, IP business case, acquisition strategy document, and request for proposal (RFP) technical package.



CHAPTER 4:

11 Myths About OpenVPX and the SOSA Initiative

MICHAEL MUNROE, Technical Product Specialist, Elma Electronic Inc.

The DoD's Hardware/Software Convergence Initiative, an effort to develop a common modular hardware architecture across defense systems using OpenVPX as its basis, is now under the aegis of the Sensor Open Systems Architecture. However, myths persist about OpenVPX.

Paradigm shifts in technology initiatives don't come without their skeptics, as is the case with the DoD's Hardware/Software Convergence Initiative. Aimed at developing a common, modular hardware architecture across C4ISR and EW systems, this program combines separate efforts initially undertaken by the U.S. Army under CERDEC (CMOSS), the U.S. Navy under NAVAIR (HOST), and the Air Force under AFLCMC into one, cohesive COTS-based, open standards initiative.

Now managed entirely under Sensor Open Systems Architecture (SOSA), this collection of open architecture standards provides reconfigurable, upgradable, and cost-effective C4ISR capabilities in deployed platforms across sensor applications throughout all major military branches. Using OpenVPX as its basis, it's setting the standard for interoperable systems across several defense branches to improve subsystem SWaP, enable rapid technology insertion, and promote reuse.

It's important to understand how both OpenVPX's history in military environments as well as its pedigree as a ratified industry standard can help facilitate this widespread, and seemingly complex, undertaking to break from the old method of costly proprietary computing systems.

Below, some common misconceptions about OpenVPX are dispelled, and we examine how it can provide the right environment for the SOSA initiative

1. The card isn't going to be compatible.

This depends on whether the target backplane is a VITA 65.0 standard development backplane or a customer-driven deployed backplane. The VITA 65.0 standard development backplanes have very simple topologies that are compatible with lots of cards. Actual VPX system backplanes have much more complex topologies with many I/O signals.

This 3U OpenVPX backplane, which serves as an integration platform for modules addressing the DoD's CMOSS initiative, provides the foundation to create systems optimized for performance, with reduced SWaP and lower lifecycle costs for rapid technology insertion.

Consequently, these backplanes are usually designed for specific cards and map to the unique I/O mapping of one VPX module. With the development of fully defined SOSA VPX slot profiles, even complex backplanes will be wired for standard slot profiles, and the result will be more modules compatible with any given backplane implementation.

2. I won't be able to get enough power.

Enough power is no longer the problem—it's properly cooling the amount of available power. In the past, VME64x and CompactPCI cards could each typically draw no more than 150 W from a backplane slot. As large FPGA silicon became available from companies such as Xilinx and Altera, the power needs of an individual card exceeded the amount of power that a card could draw because the pin assignments and contact design did not allow for more power.

3U VPX cards can draw over 270 W and 6U cards could draw over 380 W. It's unlikely that VPX systems will ever be limited due to power availability. And, new cooling standards are being released to allow more of this VPX power to be used in future systems.

3. I'll need a custom backplane.

One of the main criticisms of the VPX architecture, and a fair one at that, is that it doesn't consider all of the other VPX features that have made the architecture so desirable. The mandate for custom backplanes is, therefore, being tolerated by designers.

A new solution designed to meet the need for fully customized VPX backplanes is on the horizon. Pioneered by hard-working technical groups under SOSA, emerging standard profile definitions will eliminate much of the need for VPX backplane slots to be wired for specific, unique VPX modules when using SOSA conforming plug-in cards *(see figure)*.

4. I can't run 10 Gb/s out of the backplane.

For some time, PCIe Gen2 and 10GBase-KX4 were thought to be the fastest protocols that could be reliably passed to I/O devices through cables, which plugged into VPX backplane RTM connectors. Recently, a new approach that utilizes new backplane

materials, together with improved via design, has pushed this limit to PCIe Gen3 and 40GBase-KR4. It's highly likely that a new, backward-compatible VPX connector may even allow these higher speeds to be exceeded in the near future.

5. VITA 65 may not meet all my design needs.
This was most likely said by those who haven't reviewed the current list of available features added to VPX. In fact, it's hard to imagine an application that could not be implemented within the standard. VPX is rugged and supports two card sizes. Some of the new features include miniature coaxial backplane feed-thru, backplane optical ribbons, radial clocks, 25-Gb/s channels, rugged vibration-resistant connectors hybrid topologies, XMC sockets, as well as VITA 57.4 FPGA mezzanines that support 28-Gb/s links between the base board and the mezzanine. The coaxial modules now available are causing an explosion of new applications.

6. All of the VPX connectors are expensive because they are sole-sourced.
OpenVPX was built specifically with the goal of eliminating single-source pitfalls. To date, there are three suppliers of intermatable backplane connectors, one of which already offers three different versions of the VITA 46 connector. All versions are forward and backward-compatible.

The connectors cost more because of the performance they provide. These high-density, high-speed connectors allow space for XMC/PMC mezzanine sockets and fit within the 3U and 6U 160 Eurocard packaging formats. In addition, there are space-qualified, high-vibration-resistant, footprint-compatible VPX backplane/daughtercard connectors. Paying for the benefits of performance enhancement is true for whatever architecture you choose.

7. The multi-connector is limited to 12 Gb/s.
Although the current connector supports signaling up 12 Gb/s, which is just beyond PCIe Gen3 and 10Base-KR Ethernet, a new backward-compatible version of the same MultiGig connector is being standardized and will support Ethernet lanes up to 25 Gb/s and Fat Pipes (FP) supporting 100GBase-KR4. This connector is both backward- and forward-compatible, so that old cards can be used in the new backplanes and new cards will be usable in the old backplanes. However, the speed will always have to be negotiated down to the least capable element in the path.

8. I can't inspect VITA 66.1/66.4 optical modules in the field.
There's now an inspection card for 6U VPX conduction-cooled chassis that will automatically both inspect—and clean—VITA 66.1 optical modules installed in either the J3 or J6 position in a 6U VPX backplane.

Independent of the VPX system, this tool is tethered to a laptop running software that will execute multiple inspect/clean/inspect cycles until all of the fibers meet inspection requirements. Then, a new card can be inserted into the fully inspected VPX slot in the field. The hope is that this equipment will be extended to 3U VPX slots that are either in accordance with AV 48.1 or AV 48.2.

9. Isn't air flow-through the same as convection cooling?
Not at all. Three different cooling methods are actually included in OpenVPX that all depend on forced air. While technically not "new," since these methods have been used

with VME for years for demanding applications, they're now standardized. Check out VITA 48.5, 48.7, and 48.8. Each offer advantages over conventional forced air, because each method allows air to be directed specifically where it's needed.

10. I heard that the VITA 46.11 IPMI-based system manager isn't really secure enough for cybersecurity.

Your concerns have been heard, and the HOST and SOSA working groups are really beefing up the System Management approach and adding new capabilities, such as large file transfer support and IPMI 2.0 security. These two working groups are supported by a large team at the University of Georgia Research Institute, the U.S. Army, U.S. Air Force and NAVAIR, as well as individual companies and SBIR (Small Business Innovation Research) award winners. It's a level of cooperation never seen before.

11. Can an intermediate frequency be shared between radio cards in a VPX backplane? I've heard that there isn't sufficient isolation.

It's true that the MultiGig signal pins may not provide sufficient isolation between pairs to distribute an intermediate frequency between radio cards. However, VPX slots now support a variety of coaxial interfaces that can distribute an intermediate frequency or very precise clocks such as Precision Time Protocol (PTP) and Network Time Protocol (NPT).

VITA 67.3 only defines the opening in the backplane, the mounting holes, and alignment pins, and supports several sizes of modules as well as a growing number of unique contact configurations, including mixed coax and optical interfaces. These 67.3 modules are easily removed and replaced on the backplane, so reconfiguration is possible.

VITA is working to standardize additional contacts, but users are already employing coaxial contacts such as SMPM (multiple suppliers), nanoRF (TE currently), and SMPS (SVmicro). SMPM (many vendors) is lower density, but it supports the greatest variety of backside cable options including flexible, semi-rigid, and right-angle terminations. Some SMPM configurations are already standardized within VITA documents.

We're only addressing the backplane side because 67.3 was developed to support direct launch from the daughtercard mezzanines, though cable can also be used. Furthermore, VITA 67.3 modules can support new higher-density nanoRF and SMPS contacts. Half-size 67.3 modules with as many as 12 coaxial contacts are already in the marketplace and being used. The denser connectors only support flexible cables presently. These can be used to distribute the precision clocks already mentioned. You can also see a mix of SMPM and either nanoRF or SMPS contacts as well as optical MT ferrules combined in a single 67.3 module.

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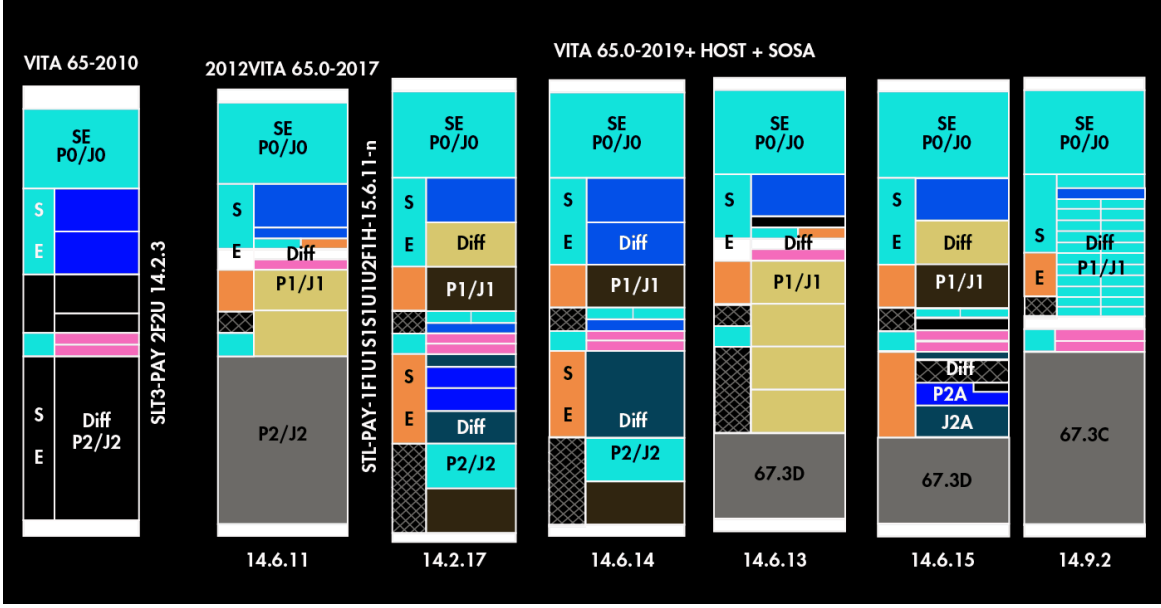


CHAPTER 5:

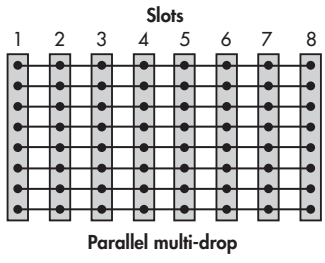
New Standard Redefines VPX Slots

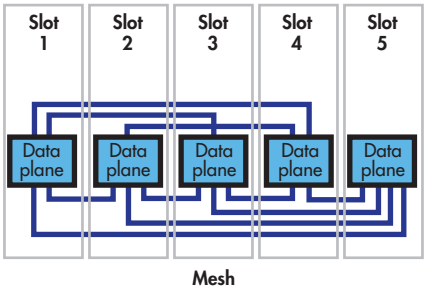
WILLIAM WONG, Editor, Electronic Design

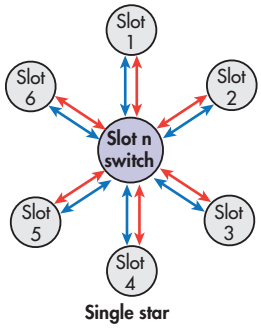
VPX standards have helped standardize many high-speed serial backplane designs, but support for arbitrary interfaces still demanded custom backplanes—until now.

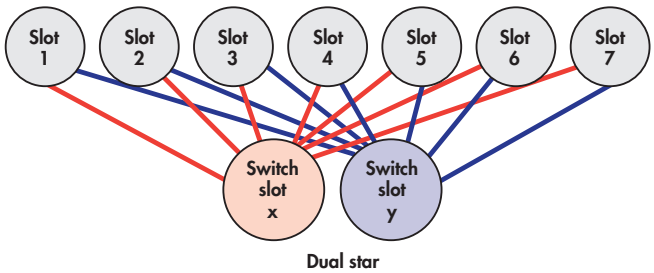
Rugged systems are crucial in the military and avionics spaces. Targeting them with commercial off-the-shelf (COTS) systems can help reduce the cost and increase the number of tools designers have to create new systems.

In the age of parallel buses, the types of backplanes and boards were significantly easier to integrate because of the more limited number of configuration options needed to address a wide range of solutions. High-speed serial interfaces have replaced



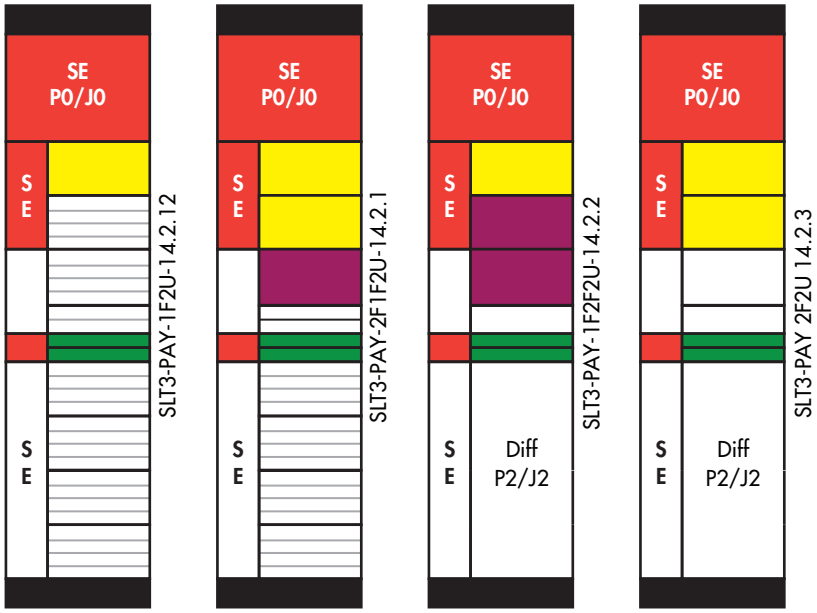






1. Parallel bus systems like ISA and PCI allow for a single backplane architecture, but point-to-point systems like Ethernet and PCI Express have multiple possible configurations. This, of course, adds complexity to backplane design. (Courtesy of Elma Electronics)

2. VITA VPX standards did define some of the board's backplane connections, but left much of it up to the designer.



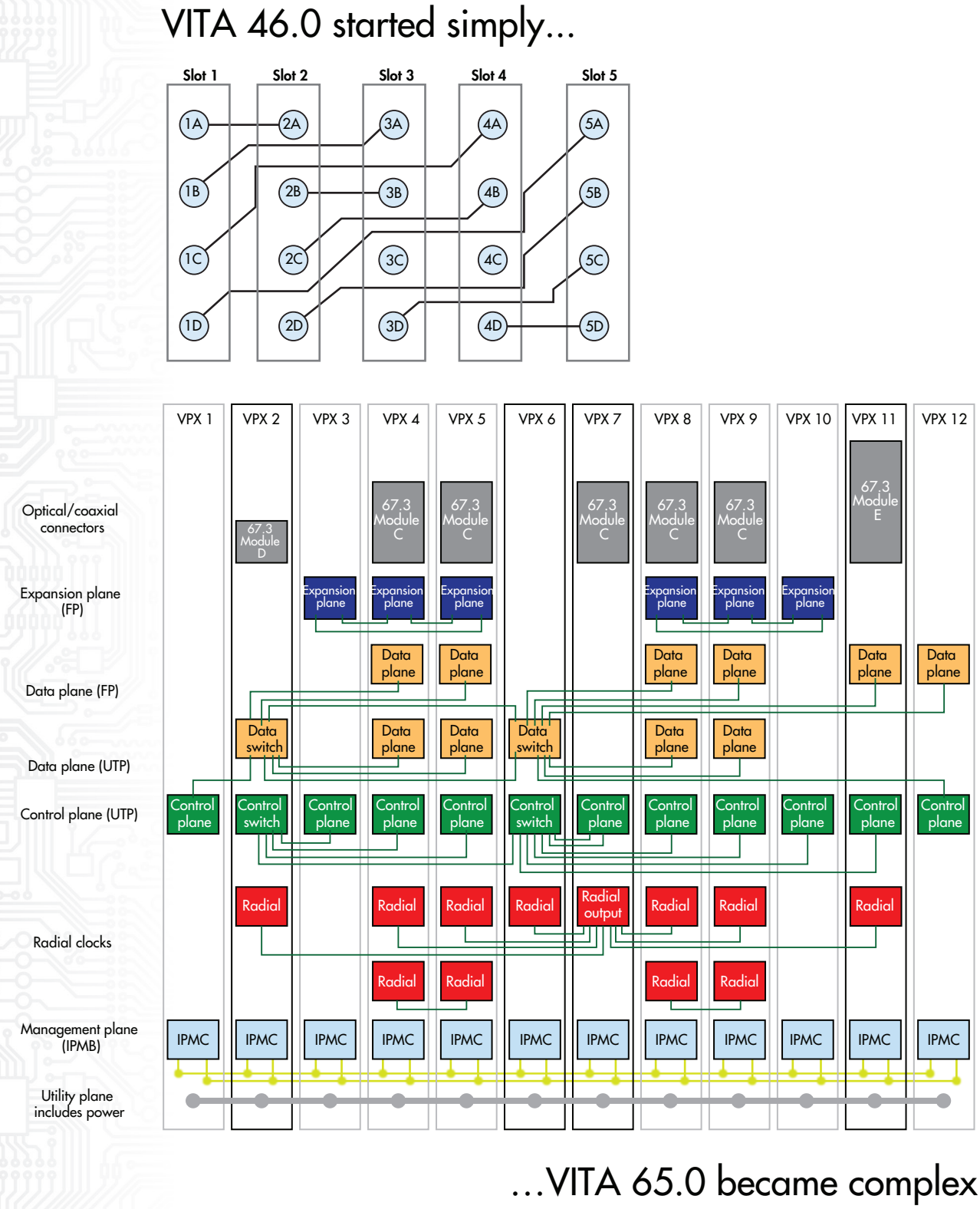
parallel interfaces,
but these are point-to-point and require much different backplane connectivity solutions *(***Fig. 1).**

VITA's VPX standards have helped standardize a significant number of high-speed serial backplane designs *(***Fig. 2)**. Unfortunately, support for arbitrary interfaces on the P1 and P2 connectors still forced the use of custom backplanes.

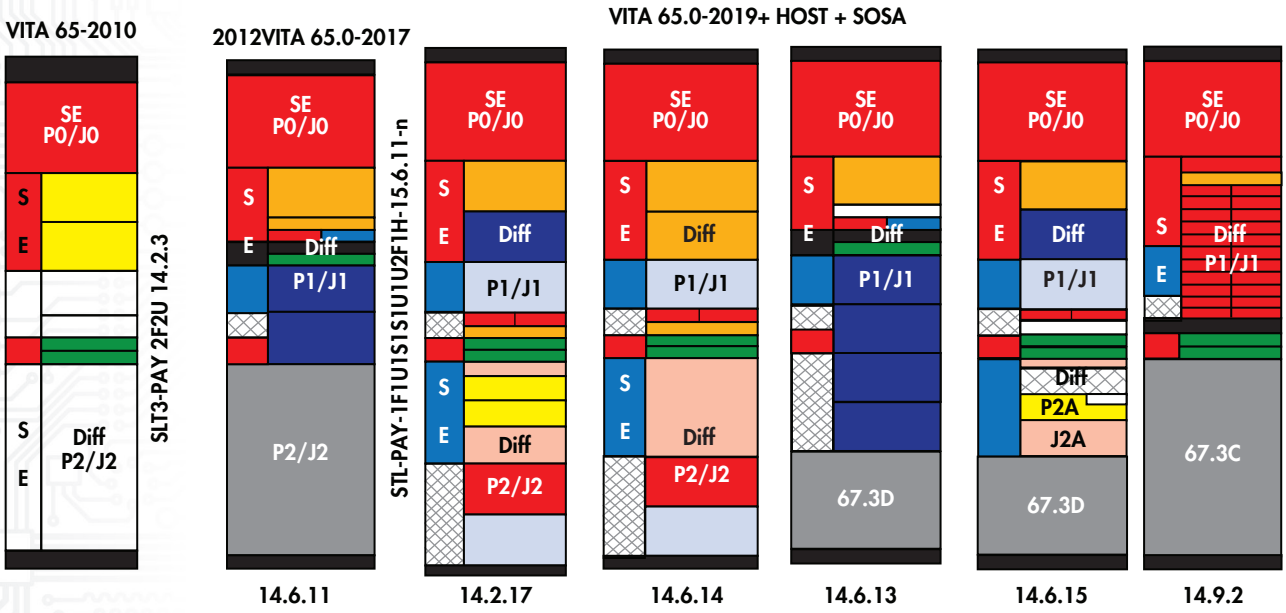
The P0 connector would contain the interface connections for PCI Express or Ethernet. VITA 46 allowed for the implementation of a full mesh network employing five slots and direct connections between each slot **(Fig. 3 on next page)**. VITA 65.0 went on to define more complex configurations using more signals. It also included management support using an IPMI bus.

The latest VITA 65 slot-profile definitions address specific configurations that define most or all of the pins, enabling backplanes to match the type of board that will work with a slot. These target different board types, such as processor boards and interface boards. Some definitions include VITA 67 RF connectors **(Fig 4 on page 19)**.

The Hardware Open Systems Technology (HOST) and Sensor Open Systems Architecture (SOSA) committees are working with the VITA Standards Organization (VSO) to create these new, fully defined slot profiles. The end result from having more standardized slots and boards will be a greater array of options for developers and increased standardization of platforms. The approach is being fostered by all three branches of the U.S. military, which is only one group that will benefit from these standards.



3. VITA 46.0 defined simple backplane connections where only communication links were involved. VITA 65.0 implementations were quite a bit more complex.



4. Currently in the queue for VITA 65.0 are slots that have most of the connections defined. This makes it possible for board and backplane vendors to deliver interchangeable solutions.

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